REMARKS

1. Claim 1 was rejected under 35 U.S.C. 102 over Roth et al., U.S. patent 5,543,339.

Claim 1 is supported by the original disclosure as follows:

> (a) forming ... first conductive gates **(select gates 144S in Figs. 3B, 18A)** ..., the first conductive gates being spaced from each other and not electrically interconnected **(at the stage of Fig. 18A)**;
>
> (b) forming ... conductive floating gates **(FG 120)** ...;
>
> (c) forming ... conductive gate lines **(control gate lines CG 134, Figs. 3A, 3B, 3F)** each of which provides second conductive gates for one column of the memory cells ...;
>
> (d) forming at least one conductive line **(WL 144, Fig. 3B)** electrically interconnecting two or more of the first conductive gates.

Claim 1 is not limited to the embodiments discussed herein.

The Examiner states:

> Roth et al. shows ... first conductive gates 52 ... conductive floating gates 13 ...

Roth's numeral 52 denotes a cavity in a floating gate 51. See Roth's Abstract and Fig. 6. Roth's member 13 is part of floating gate 51 (column 3, last sentence). Cavities 52 are thus not conductive gates, but cavities 52 are completely or partially filled with the material of word lines 91 which provide control gates (column 4, lines 42-53; column 5, lines 4-6).

The Examiner states that Roth discloses "forming at least one conductive line 91 electrically interconnecting two or more of the first conductive gates". Roth indeed discloses word line 91 providing the control gates, but Roth does not disclose a processing stage in which the individual control gates are not electrically interconnected as recited in paragraph (a) of Claim 1. Roth's layer 91 is deposited and patterned as described in column 4, lines 42-45. The deposition process provides both the control gates and the word line portions

interconnecting the control gates, and there is no teaching or suggestion to form the control gates before the interconnecting portions.

2. Claims 2-10 were rejected under 35 U.S.C. 103(a) over Roth. The rejection is assumed to apply only to Claims 2-9 because Claim 10 is shown as objected to.

Claims 2-9 depend from Claim 1, and are believed to be allowable because Roth does not teach or suggest separate formation of the control gates and the wordline portions interconnecting the control gates as discussed above in connection with Claim 1. Additional reasons for some of these claims are as follows:

Claim 2 recites that the first conductive gates are formed **before** the floating gates. In Applicant's Fig. 3B, select gates 144S are formed before floating gates 120. The floating gate fabrication is shown in Figs. 19-27A. Some of the advantages due to this fabrication order in this embodiment are explained in Applicant's specification, page 3, lines 5-7 (the floating gates are not affected by the fabrication of select gate dielectric). Claim 2 is not limited to the embodiments and advantages discussed herein.

In Roth, control gates 91 are formed **after** the floating gates 51, which is the opposite from Applicant's invention. Moreover, since the control gates 91 are formed simultaneously with the word lines, and the word lines at least partially fill floating gate cavities, Roth suggests that the floating gate cavities, and hence the floating gates themselves, must be fabricated before the control gates, and thus teaches away from forming the control gates before the floating gates as recited in Claim 2.

The same applies to Claims 3-4.

Claim 7 recites that "the first conductive gates comprise a semiconductor material, and the conductive line is a metal line".

Roth's control gates 91 are fabricated simultaneously with the lines interconnecting the control gates. Therefore, if the lines 91 were metal lines then the control gates would have to be metal gates.

3. Claims 1-11 and 25-32 were rejected for obviousness type double patenting. A terminal disclaimer is attached to overcome the rejection.

Any questions regarding this case can be addressed to the undersigned at the telephone number below.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 19, 2005.

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